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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,731	SONG, HO UK	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is responsive to the amendment filed on 03-18-05. Applicant's arguments with respect to reference Watkins have been carefully considered but they are not deemed to be persuasive to overcome the references. Thus, the claims remained rejected under Watkins. New ground of rejections necessitated by the amendment is set forth below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 3, 4, 8 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Claims 2, 4, 8 and 13 are indefinite because it is misdescriptive. None of the drawing shows that the off –chip drivers can perform NAND operation when the control signal is high and when the control signal is low, the off-chip drivers perform NOR operation. For instance the circuit of figure 3 of the present application performs as NAND function when the control input is HIGH. When the control input is LOW, the output is always high. The circuit of figure 4 performs as an inverter when the control input is HIGH and when the control input is LOW, the output is always LOW. Clear explanation is required.

Regarding claim 3, the recitation "a plurality of off-chi drivers ...generating a plurality of output signals ...the delay circuits respectively receive the output signals..." is indefinite because it is misdescriptive. Figure 2 of the present application shows that the off-chip drivers receive the delayed DATA signals and the delay circuits receive the input DATA signal and generate delayed DATA signals.

Regarding claim 5, the recitation " wherein a total drivability of the off-chip driver is at least 80% of a target drivability" is indefinite because it is not clear what the "80% of a target drivability" is meant by.

Regarding claim 11, the recitation " the output driver circuit connected to the output terminals of the delay circuits and the pre-drive circuit" on lines 8-9 is indefinite because it is misdescriptive. Figure 2 of the present application shows that the output driver circuit (300) is connected to the outputs of the off-chip drivers.

Regarding claim 14, the recitation "the output driver circuit comprises output drivers connected to output terminals of the delay circuits" is indefinite because it is misdescriptive. Figure 2 of the present application shows that the output driver circuit is connected to the output terminals of the off-chip drivers.

Claims 12 and 15 are indefinite because are indefinite because of the technical deficiencies of claims 11.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Watkins et al (USP. 6,359,483),

Regarding claim 1-5, figure 2 of Atkins shows an off-chip driver comprising: plurality of delay circuits (128), combination of (128) and (13), (128, 130,132) etc, (note that the combination of the buffers forms parallel delay circuits that receive a same data input signal which can be a clock data signal), a plurality of off chip drivers (144-154) receiving the delayed data and controlled by different control signals generated from the control circuit comprising elements (112-120). The number of the off-chip driver is activated in response to the control signals.The off chip drivers are NAND gates. The delay circuits have different delay times (D, 2D, 3D...) depending on the combination of the buffers (128-140) and the delay circuits receive a same input. Depending on the load requirement, inherently the off-chip drivers are turned on depending on the load requirement (80% etc...). The output driver is the multiple inputs NAND gate.

Regarding claims 6 and 8, figure 2 of Watkins shows a data output circuit comprising a plurality of delay circuits in parallel (128), (128 and 123), (128, 139, 132)... , a plurality of off-chip drivers (144-154), a pre-driver circuit (142) receiving the input clock data. The output driver circuit (the multiple input NAND) connects the output terminals of the off-chip drivers (144-154) and the pre-driver circuit (142). The off-chip drivers are activated by control signals (the output of flip-flops).

Regarding claim 7, the output of the pre-driver (142) is a NAND gate. The output signal of the pre-driver is high or low (pull-up/pull-down) depending on the logical status of the input data clock signal.

Regarding claim 9, the control signals applied to the off-chip drivers (144-154), the outputs of the off-chip drivers activate the output driver circuit (the multiple input NAND). An output driver internal to the output driver circuit is activated to output data output signal (B).

Regarding claim 10, it is inherent that the drivability of the off-chip driver is selected (designed) to driver the load (target) depending on the load requirement.

Regarding claims 11-13, figure 2 of Watkins shows a data output circuit comprising a plurality of off-chip drivers (144-154), a plurality of parallel delay circuits (128), (128 and 123), (128, 139, 132)..., a pre-driver circuit (142). The output driver circuit (the multiple input NAND gate) is connected to the output terminals of the off-chip drivers (144-154). The pre-driver circuit (142) receives the data clock signal and performs a pull-up or pull-down function (the output of the pre-driver circuit is high or low depending on the data signal. The off-chip drivers comprise NAND gates.

Regarding claims 14 and 15, the output driver circuit (multiple inputs NAND gate) comprises internal output drivers. When the control signal of an off-chip driver is enabled, an internal transistor of the off-chip driver is enabled (driven). The off-chip drivers are designed to drive the output load (target). Depending on the load requirement, inherently the off-chip drivers are turned on the meet the load requirement.

Claims 1, 3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirasaka (USP. 6,134,691).

Regarding claims 1, 3 and 5, figure 5 of Hirasaka shows an off-chip driver circuit comprising: a plurality of parallel delay circuits (DL1-DL2) having different delay values and receiving a data signal, a plurality of off-chip drivers (S0-S2) for receiving a data signal and generate delayed data signals in response to respective control signals. The number of off-chip driver to be activated is changed from 0-N (N=2). Depending on the load requirement, inherently the off-chip drivers are turned on the meet the load requirement (60%. 80%...).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-5251.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
06-06-05

TUAN T. LAM
PRIMARY EXAMINER